Ferroelectric Tunnel Junction Optimization by Plasma-Enhanced Atomic Layer Deposition

[[1]](#footnote-1)

Jae Hur, Yuan-Chun Luo, Panni Wang, Nujhat Tasneem, Asif Islam Khan and Shimeng Yu

*Abstract*— Ferroelectric tunnel junction (FTJ) based on doped/alloyed HfO2 and ZrO2 is emerging as a promising candidate for the crossbar array for high density memory and compute-in-memory. FTJ is able to operate under non-destructive read mechanism as opposed to the ferroelectric capacitor. However, due to the low on/off ratio and small read-out current of the tunneling mechanism, the integration HZO-based FTJs with CMOS peripheral sensing circuitry is challenging. Herein, we report an optimized fabrication process that boosts the on-state current while suppressing the off-state current leading to an improved performance in Hf0.5Zr0.5O2 (HZO) based FTJs. The plasma-enhanced atomic layer deposited (PEALD) of HZO and the incorporation of an interlayer Al2O3 are keys to improve the HZO-based FTJ in terms of the on/off ratio and cycling endurance.

*Index Terms*—Ferroelectric tunnel junction (FTJ), plasma-enhanced atomic layer deposition (PEALD), remnant polarization (*P*r), thermal atomic layer deposition (THALD)

# INTRODUCTION

T

he ferroelectric tunnel junction (FTJ) is an emerging device that has recently obtained considerable attention in wide-range applications from high density memory to compute-in-memory device [1]–[11]. Compared to other intensively studied three-terminal devices such as ferroelectric field-effect-transistor (Fe-FET) [12]–[14] or ferroelectric random access memory (FeRAM) [15], [16], FTJ is a two-terminal device that is suitable for crossbar array. Since the discovery of ferroelectricity in doped/alloyed HfO2 and ZrO2 thin films with post-deposition annealing for crystallization, researchers have investigated process optimizations of the material composition and annealing temperature to improve the quality of HZO based ferroelectrics [17]–[19]. It is noteworthy that HfO2 and ZrO2, the composing elements of the HZO film, have been the most favorably utilized materials in semiconductor industry thanks to their superior compatibility with the silicon fabrication processes. Though HZO-based FeFET and FeRAM are more mature technologies today, HZO-based FTJ has been drawing great attention recently due to its interesting features such as non-destructive read mechanism along and low power operation. There have been two different structural flavors to the FTJ stack, one with interlayer (IL) [3], [9], [11] and the other without IL [1], [2], [4]–[8], [10] adjacent to the ferroelectric layer. The former one has several merits over the latter in that: (i) it has intrinsic diode characteristics, which allows the FTJ to be able to be integrated into crossbar array without additional selector device [3], (ii) it can solve the problem of symmetry of the FTJ layers that leads to reduced tunneling coefficient [11], and (iii) higher remnant polarization (*P*r) can be obtained by stacking thicker ferroelectric film [20]. However, the remaining challenges for HZO-based FTJ include low on/off ratio and small read-out current.

In this work, Hf0.5Zr0.5O2 (HZO) based FTJs with two different fabrication techniques (thermal atomic layer deposition, THALD and plasma-enhanced atomic layer deposition, PEALD) are systematically compared. It was found that the on/off ratio and cycling endurance characteristics showed much improved performance using PEALD for the layers of IL and HZO. To the best of our knowledge, it is the first time that an FTJ device fabricated with PEALD is demonstrated with its improved performance compared to prior works using THALD. It is also noteworthy that the entire stack of the FTJ including the electrode was deposited *in*-*situ* without breaking the vacuum.

# Results and Discussion

**Fig. 1(a)** shows the basic FTJ structure composed of separate layers of TiN, Al2O3, and HZO for top/bottom electrode, IL, and ferroelectric barrier respectively. The TiN layer was deposited with PEALD with thickness of 20 nm while Al2O3 and HZO were deposited either with THALD or PEALD. The precursors of TMA was used for Al2O3 with 2 nm and TDMA-Hf and TDMA-Zr were used for HZO with 10 nm. This entire stack was deposited without breaking the vacuum in the Fiji G2 system at 250 oC. Afterwards, the stack was annealed at 450 oC for 30 s and then the top metal pad of Al layer was deposited with e-beam evaporator with 100 nm. Finally, the top metal pad and electrode were patterned and wet-etched. The fabrication process flow is shown in **Fig. 1(b)**. **Fig. 1(c)** and **(d)** demonstrate the quantitatively sketched energy band diagram of the FTJ when it is in the off-state and on-state. The thin and thick arrows in the figures represent the small and large tunneling current flowing through the effective energy barriers. In this work, two types of FTJ devices were fabricated, one with Al2O3 and HZO layers by THALD and another one using PEALD. For polarization response test, the aixACCT TF-3000 ferroelectric parameter analyzer was used while dynamic leakage current compensation mode was off. **Fig. 2(a)** and **(b)** show the typical polarization-voltage (P-V) characteristics of the entire FTJ stack (after a wake-up process of high electric field of ±7.0 MV/cm) with sweeping voltage from ±3.5 V to ±7.0 V with 0.5 V increment. The remnant polarization (*P*r) and saturation polarization (*P*s) are rather comparable between the two FTJs. The leakage is, however, severely noticeable for the THALD FTJ in the P-V loop when compared to the PEALD FTJ as voltage increases. This can be correlated with the electrical breakdown properties of the THALD and PEALD HZO-only thin films sandwiched between top and bottom electrodes of TiN, as in **Fig. 3(a)**. The breakdown electric-field (*E*BD) is larger and also the off-state leakage is lower for the PEALD HZO when compared to THALD HZO. The plasma O2 gas used in PEALD is able to form a clearer crystalline structure with metastable ferroelectric phases, which is considered to be the reason of stronger dielectric property for PEALD HZO than that for THALD HZO [21]. **Fig. 3(b)** displays the P-V endurance characteristics of the THALD and PEALD HZO capacitor with electric field stress (*E*pulse) of ±2.5 MV/cm and using triangular pulse with pulse width (*t*pulse) of 1 ms. It can be observed that the cycling wake-up process is more prominent for the THALD HZO while the PEALD HZO showed almost no wake-up cycles and stayed rather stable. Moreover, the THALD HZO shows severe fatigue effect right after it experiences the wake-up cycles of 1000. These polarization characteristics demonstrated in **Fig. 2** and **3** can be directly related to the FTJ performance as discussed in [13]. For erase (to off-state) and program sequence (to on-state) of the FTJ devices, 6 V and -4 V, with pulse widths of 50 μs and 10 μs respectively, have been applied to the top Al pad using Keithley 4200-SCS. It was found that further increase of program voltage does not increase the on/off ratio but only reduces the endurance cycles. Larger positive voltage and time were needed for erasing because the current is much lower when attempting to turn the device off from the on-state, which can be understood due to the asymmetry in the stack as shown in **Fig. 1(c)** and **(d)**. The read voltage of the FTJs was chosen to be 1.5 V which does not generate significant trap sites, and also resulted in the reasonable on/off ratio. In **Fig. 4**(a), the on/off characteristics of the THALD and PEALD FTJs are shown. The on/off ratio is higher for PEALD FTJ through the endurance cycling. In **Fig. 4(b)**, the *I*ON increases significantly after experiencing approximately 100s of cycles in THALD FTJ from the beginning, which is correspondent to wake-up characteristics of the P-V endurance curve in **Fig. 3(b)**. Considering the relatively small read voltage we used, the on-current (*I*ON) of approximately 10 μA/cm2 for PEALD FTJ is comparable or even higher than previous literature data [4], [11], [22]. In **Fig. 4(c)**, the off-current (*I*OFF) behavior is shown and it is larger for THALD FTJ owing to its less strong dielectric property as demonstrated in **Fig. 2(a)** and **Fig. 3(a)**. Thus, THALD FTJ results in lower on/off ratio along with rather lower *I*ON. Note that on/off ratio of the PEALD FTJ in this work reaches over 120%, which is the highest value obtained when compared with the HZO-based FTJs except [5] where epitaxial growth technique was utilized. All of these FTJ performance can be understood via the current characteristics of the FTJ in **Fig. 5**. In **Fig. 5(a)** and **(b)**, from 10 to 100 cycles indicated as A, A’, B and B’, the wake-up effect can be observed for both FTJs at the negative and positive voltages. The peak current value is both larger in PEALD FTJ, which can explain the higher on/off ratio in **Fig. 4(a)**. Indicated with C, from 100 to 2000 cycles, the fatigue effect in THALD FTJ attributes to the lower *I*ON as well in **Fig. 5(a)**. The exponentially increasing *I*OFF, as the number of cycles increases for THALD FTJ, can be understood with arrow of D. Finally, it is concluded that both the *I*ON and *I*OFF could be improved using PEALD process for FTJ, which are correspondent to their ferroelectric properties, *i*.*e*., P-V and I-V characteristics.





Fig. 1. (a) Device structure and (b) fabrication process flow of the HZO-based FTJ, (c) off-state and (d) on-state energy band diagram of the FTJ.



Fig. 2. P-V characteristics of (a) THALD FTJ and (b) PEALD FTJ.



Fig. 3. (a) Current density-electric field characteristics and (b) endurance characteristics of THALD and PEALD HZO films.



Fig. 4. (a) On/off ratio, (b) on-current and (c) off-current of the THALD and PEALD FTJs with two representative cells.



Fig. 5. Current characteristics of (a) THALD FTJ and (b) PEALD FTJ with cycling endurance.

# Conclusion

This work demonstrated two types of FTJ devices, where THALD and PEALD have been used in the fabrication process. The FTJ performance in terms of on/off ratio has been compared between the two FTJs with respect to the cycling endurance. It was found that the FTJ with PEALD exhibits boosted on/off ratio along with better cycling endurance. Most importantly, device performance of the FTJs was explained corresponding to not only P-V but also the I-V characteristics. For the suppressed *I*OFF, it could be explained with the stronger dielectric property of the more crystallized PEALD HZO layer having lower leakage and higher *E*BD. The higher *I*ON from the PEALD FTJ is attributed to the relatively higher *P*r value and its non-fatiguing behavior. Since it is the first time to demonstrate the enhanced performance of PEALD HZO-stacked FTJs, this work will shed light on improvement of FTJ devices in the future research.

References

[1] A. Chernikova *et al.*, “Ultrathin Hf0.5Zr0.5O2 ferroelectric Films on Si,” *ACS Appl. Mater. Interfaces*, vol. 8, no. 11, pp. 7232–7237, Mar. 2016, doi: 10.1021/acsami.5b11653.

[2] Z. Fan *et al.*, “Ferroelectricity and ferroelectric resistive switching in sputtered Hf 0.5 Zr 0.5 O 2 thin films,” *Appl. Phys. Lett.*, vol. 108, no. 23, p. 232905, Jun. 2016, doi: 10.1063/1.4953461.

[3] S. Fujii, Y. Kamimuta, T. Ino, Y. Nakasaki, R. Takaishi, and M. Saitoh, “First demonstration and performance improvement of ferroelectric HfO2-based resistive switch with low operation current and intrinsic diode property,” in *2016 IEEE Symposium on VLSI Technology*, 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573413.

[4] F. Ambriz-Vargas *et al.*, “A Complementary Metal Oxide Semiconductor Process-Compatible Ferroelectric Tunnel Junction,” *ACS Appl. Mater. Interfaces*, vol. 9, no. 15, pp. 13262–13268, Apr. 2017, doi: 10.1021/acsami.6b16173.

[5] H. Y. Yoong *et al.*, “Epitaxial Ferroelectric Hf0.5Zr0.5O2 Thin Films and Their Implementations in Memristors for Brain-Inspired Computing,” *Advanced Functional Materials*, vol. 28, no. 50, p. 1806037, 2018, doi: 10.1002/adfm.201806037.

[6] Z. Dong, X. Cao, T. Wu, and J. Guo, “Tunneling current in HfO 2 and Hf 0.5 Zr 0.5 O 2 -based ferroelectric tunnel junction,” *Journal of Applied Physics*, vol. 123, no. 9, p. 094501, Mar. 2018, doi: 10.1063/1.5016823.

[7] M. Kobayashi, Y. Tagawa, F. Mo, T. Saraya, and T. Hiramoto, “Ferroelectric HfO2 Tunnel Junction Memory With High TER and Multi-Level Operation Featuring Metal Replacement Process,” *IEEE Journal of the Electron Devices Society*, vol. 7, no. 1, pp. 134–139, 2019, doi: 10.1109/JEDS.2018.2885932.

[8] Y. Goh and S. Jeon, “The effect of the bottom electrode on ferroelectric tunnel junctions based on CMOS-compatible HfO2,” *Nanotechnology*, vol. 29, no. 33, p. 335201, Jun. 2018, doi: 10.1088/1361-6528/aac6b3.

[9] R. Berdan *et al.*, “In-memory Reinforcement Learning with Moderately-Stochastic Conductance Switching of Ferroelectric Tunnel Junctions,” in *2019 Symposium on VLSI Technology*, 2019, pp. T22–T23, doi: 10.23919/VLSIT.2019.8776500.

[10] B. Mittermeier *et al.*, “CMOS Compatible Hf0.5Zr0.5O2 Ferroelectric Tunnel Junctions for Neuromorphic Devices,” *Advanced Intelligent Systems*, vol. 1, no. 5, p. 1900034, 2019, doi: 10.1002/aisy.201900034.

[11] B. Max, M. Hoffmann, S. Slesazeck, and T. Mikolajick, “Direct Correlation of Ferroelectric Properties and Memory Characteristics in Ferroelectric Tunnel Junctions,” *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 1175–1181, 2019, doi: 10.1109/JEDS.2019.2932138.

[12] H. Mulaosmanovic *et al.*, “Novel ferroelectric FET based synapse for neuromorphic systems,” in *2017 Symposium on VLSI Technology*, 2017, pp. T176–T177, doi: 10.23919/VLSIT.2017.7998165.

[13] M. Jerry *et al.*, “Ferroelectric FET analog synapse for acceleration of deep neural network training,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 6.2.1-6.2.4, doi: 10.1109/IEDM.2017.8268338.

[14] M. Seo *et al.*, “First Demonstration of a Logic-Process Compatible Junctionless Ferroelectric FinFET Synapse for Neuromorphic Applications,” *IEEE Electron Device Letters*, vol. 39, no. 9, pp. 1445–1448, Sep. 2018, doi: 10.1109/LED.2018.2852698.

[15] J. S. Yoon, A. Tewari, C. Shin, and S. Jeon, “Influence of High-Pressure Annealing on Memory Properties of Hf0.5Zr0.5O2 Based 1T-FeRAM,” *IEEE Electron Device Letters*, vol. 40, no. 7, pp. 1076–1079, Jul. 2019, doi: 10.1109/LED.2019.2918797.

[16] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, “Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors,” in *2011 International Electron Devices Meeting*, 2011, pp. 24.5.1-24.5.4, doi: 10.1109/IEDM.2011.6131606.

[17] M. Hyuk Park, H. Joon Kim, Y. Jin Kim, W. Lee, T. Moon, and C. Seong Hwang, “Evolution of phases and ferroelectric properties of thin Hf 0.5 Zr 0.5 O 2 films according to the thickness and annealing temperature,” *Appl. Phys. Lett.*, vol. 102, no. 24, p. 242905, Jun. 2013, doi: 10.1063/1.4811483.

[18] S. Starschich, T. Schenk, U. Schroeder, and U. Boettger, “Ferroelectric and piezoelectric properties of Hf1-xZrxO2 and pure ZrO2 films,” *Appl. Phys. Lett.*, vol. 110, no. 18, p. 182905, May 2017, doi: 10.1063/1.4983031.

[19] S. Shibayama, T. Nishimura, S. Migita, and A. Toriumi, “Thermodynamic control of ferroelectric-phase formation in Hf  *x*  Zr  1− *x* O 2 and ZrO 2,” *Journal of Applied Physics*, vol. 124, no. 18, p. 184101, Nov. 2018, doi: 10.1063/1.5028181.

[20] B. Max, T. Mikolajick, M. Hoffmann, S. Slesazeck, and T. Mikolajick, “Retention Characteristics of Hf0.5Zr0.5O2-Based Ferroelectric Tunnel Junctions,” in *2019 IEEE 11th International Memory Workshop (IMW)*, 2019, pp. 1–4, doi: 10.1109/IMW.2019.8739765.

[21] T. Onaya *et al.*, “Ferroelectricity of HfxZr1−xO2 thin films fabricated by 300 °C low temperature process with plasma-enhanced atomic layer deposition,” *Microelectronic Engineering*, vol. 215, p. 111013, Jul. 2019, doi: 10.1016/j.mee.2019.111013.

[22] F. Ambriz-Vargas *et al.*, “Tunneling electroresistance effect in a Pt/Hf 0.5 Zr 0.5 O 2 /Pt structure,” *Appl. Phys. Lett.*, vol. 110, no. 9, p. 093106, Feb. 2017, doi: 10.1063/1.4977028.

1. This work was supported by ASCENT, one of the SRC/DARPA JUMP Centers.

   Jae Hur, Yuan Chun, Panni Wang, Nujhat Tansneem, Asif Islam Khan and Shimeng Yu are with the School of Electrical and Computing Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA (e-mails: [asif.khan@ece.gatech.edu](mailto:asif.khan@ece.gatech.edu), and [shimeng.yu@ece.gatech.edu](mailto:shimeng.yu@ece.gatech.edu)) [↑](#footnote-ref-1)